In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1   1.   (Currently Amended) A method of exporting emulation
2   information from a data processor, comprising:
3   collecting internal emulation information from a data
4   processor at a data processor clock rate;
5   arranging the collected emulation information into a plurality
6   of first information blocks having a first fixed size;
7   receiving the plurality of first information blocks and
8   arranging the emulation information contained therein into a
9   plurality of second information blocks having a second fixed size
10   which differs from the first fixed size of the first information
11   blocks; and
12   outputting a sequence of the second information blocks via a
13   plurality of terminals ~~equal in number to said second fixed size~~ at
14   a transmission clock rate, said first fixed size, said data
15   processor clock rate, said second fixed size and said transmission
16   clock rate related whereby a bit rate of first information blocks
17   equals a bit rate of said second information blocks.

1   2.   (Previously Presented) The method of Claim 1, wherein the
2   second fixed size is smaller in size than the first fixed size.

1   3.   (Original) The method of Claim 1, including receiving the
2   sequence of second information blocks externally of the data
3   processor, and re-arranging the emulation information contained in
4   the second information blocks into a plurality of the first
5   information blocks.

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1   4.   (Original) The method of Claim 1, wherein each of the
2   first and second information blocks is a packet of emulation
3   information.

        Claims 5 to 15.   (Cancelled)

1   16.   (Currently Amended) An integrated circuit, comprising:
2   a data processor for performing data processing operations;
3   a collector coupled to said data processor for collecting
4   emulation information from said data processor at a data processor
5   clock rate and arranging said emulation information into a
6   plurality of first information blocks having a first fixed size;
7   an exporter coupled to said collector for receiving therefrom
8   said plurality of first information blocks and arranging said
9   emulation information contained therein into a plurality of second
10 information blocks having a second fixed size which differs from
11 the first fixed size of said first information blocks;
12   a plurality of terminals for outputting information ~~equal in~~
13 ~~number to said second fixed size~~; and
14   said exporter coupled to said terminals for outputting a
15 sequence of the second information blocks via said terminals at a
16 transmission clock rate, said first fixed size, said data processor
17 clock rate, said second fixed size and said transmission clock rate
18 related whereby a bit rate of first information blocks equals a bit
19 rate of said second information blocks.

1   17.   (Previously Amended) The integrated circuit of Claim 16,
2   wherein said second fixed size is smaller in size than said first
3   fixed size.

        Claims 18 to 26.   (Canceled)

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1   27.   (Currently Amended) A data processing system, comprising:

2   an integrated circuit, including a data processor for

3   performing data processing operations;

4   an emulation controller coupled to said integrated circuit for

5   controlling emulation operations of said data processor;

6   said integrated circuit including an apparatus coupled between

7   said data processor and said emulation controller for providing

8   emulation information about said data processing operations, said

9   apparatus including a collector coupled to said data processor for

10   collecting said emulation information from said data processor at a

11   data processor clock rate and arranging said emulation information

12   into a plurality of first information blocks having a first fixed

13   size, and an exporter coupled to said collector for receiving

14   plurality of first information blocks and arranging said emulation

15   information contained therein into a plurality of second

16   information blocks having a second fixed size which differs from

17   the first fixed size of said first information blocks; and

18   said integrated circuit including a plurality of terminals

19   coupled to said emulation controller ~~equal in number to said second~~

20   ~~fixed size~~ for outputting information to said emulation controller,

21   said exporter coupled to said terminals for outputting a sequence

22   of said second information blocks to said emulation controller via

23   said terminals at a transmission clock rate, said first fixed size,

24   said data processor clock rate, said second fixed size and said

25   transmission clock rate related whereby a bit rate of first

26   information blocks equals a bit rate of said second information

27   blocks.

1   28.   (Original) The system of Claim 27, including a

2   man/machine interface coupled to said emulation controller for

3   permitting a user to communicate with said emulation controller.

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1   29. (Original) The system of Claim 28, wherein said
2   man/machine interface includes one of a visual interface and a
3   tactile interface.

1   30. (Currently Amended) The method of Claim 2, wherein:
2   said first fixed size is an integral multiple of said second
3   fixed size; and
4   said step of receiving the plurality of first information
5   blocks and arranging the emulation information contained therein
6   into a plurality of second information blocks includes the steps of
7   (a) storing a current first information block in a
8   current packet register,
9   (b) sequentially selecting groups of the second fixed
10   size bits from the current packet register as a second
11   information block, a first selected group beginning at a first
12   bit of said current packet register, subsequent selected
13   groups beginning at a bit following a last bit of a prior
14   group, until all bits of the current packet register are
15   selected,
16   (c) thereafter storing a next first information block in
17   the current ~~block~~ packet register and repeating steps (a), (b)
18   and (c).

1   31. (Previously Presented) The method of Claim 2, wherein:
2   said first fixed size is not an integral multiple of said
3   second fixed size; and
4   said step of receiving the plurality of first information
5   blocks and arranging the emulation information contained therein
6   into a plurality of second information blocks includes the steps of
7   (a) storing a current first information block in a
8   current packet register,

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9   (b) sequentially selecting groups of the second fixed

10 size bits from the current packet register as a second

11 information block, a first selected group beginning at a next

12 bit of said current packet register, subsequent selected

13 groups beginning at a bit following a last bit of a prior

14 group, until a number of bits of remaining in the current

15 packet register is less than the second fixed number,

16 (c) storing the current first information block in a last

17 packet register,

18 (d) storing a next first information block in the current

19 packet register,

20 (e) selecting a group of the second fixed size bits from

21 a set of bits remaining in the last packet register and bits

22 starting at a first bit of the current packet register, and

23 (f) thereafter repeating steps (b), (c), (d) and (e).

1   32. (Currently Amended) The integrated circuit of claim 17,

2   wherein:

3   said first fixed size is an integral multiple of said second

4   fixed size; and

5   said exporter includes

6   a current packet register, and

7   a combiner connected to said current packet register and

8   said terminals, said combiner operable to

9   (a) store a current first information block in a

10 current packet register,

11 (b) sequentially select groups of the second fixed

12 size bits from the current packet register as a second

13 information block, a first selected group beginning at a

14 first bit of said current packet register, subsequent

15 selected groups beginning at a bit following a last bit

16   of a prior group, until all bits of the current packet

17   register are selected,

18   (c) thereafter store a next first information block

19   in the current ~~block~~ <u>packet</u> register and repeat steps

20   (a), (b) and (c).

1   33.   (Previously Presented) The integrated circuit of claim

2   17, wherein:

3   said first fixed size is not an integral multiple of said

4   second fixed size; and

5   said exporter includes

6   a current packet register,

7   a last packet register, and

8   a combiner connected to said current packet register and

9   said terminals, said combiner operable to

10   (a) store a current first information block in a

11   current packet register,

12   (b) sequentially select groups of the second fixed

13   size bits from the current packet register as a second

14   information block, a first selected group beginning at a

15   next bit of said current packet register, subsequent

16   selected groups beginning at a bit following a last bit

17   of a prior group, until a number of bits of remaining in

18   the current packet register is less than the second fixed

19   number,

20   (c) store the current first information block in a

21   last packet register,

22   (d) store a next first information block in the

23   current packet register,

24   (e) select a group of the second fixed size bits

25   from a set of bits remaining in the last packet register

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26   and bits starting at a first bit of the current packet
27   register, and
28   (f) thereafter repeat steps (b), (c), (d) and (e).

1   34. (Previously Presented) The data processing system of
2   Claim 27, wherein:
3   said second fixed size is smaller in size than said first
4   fixed size.

1   35. (Currently Amended) The data processing system of claim
2   34, wherein:
3   said first fixed size is an integral multiple of said second
4   fixed size; and
5   said exporter includes
6   a current packet register, and
7   a combiner connected to said current packet register and
8   said terminals, said combiner operable to
9   (a) store a current first information block in a
10   current packet register,
11   (b) sequentially select groups of the second fixed
12   size bits from the current packet register as a second
13   information block, a first selected group beginning at a
14   first bit of said current packet register, subsequent
15   selected groups beginning at a bit following a last bit
16   of a prior group, until all bits of the current packet
17   register are selected,
18   (c) thereafter store a next first information block
19   in the current ~~block~~ <u>packet</u> register and repeat steps
20   (a), (b) and (c).

1   36. (Previously Presented) The data processing system of
2   claim 34, wherein:

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3   said first fixed size is not an integral multiple of said
4   second fixed size; and
5   said exporter includes
6   a current packet register,
7   a last packet register, and
8   a combiner connected to said current packet register and
9   said terminals, said combiner operable to
10   (a) store a current first information block in a
11   current packet register,
12   (b) sequentially select groups of the second fixed
13   size bits from the current packet register as a second
14   information block, a first selected group beginning at a
15   next bit of said current packet register, subsequent
16   selected groups beginning at a bit following a last bit
17   of a prior group, until a number of bits of remaining in
18   the current packet register is less than the second fixed
19   number,
20   (c) store the current first information block in a
21   last packet register,
22   (d) store a next first information block in the
23   current packet register,
24   (e) select a group of the second fixed size bits
25   from a set of bits remaining in the last packet register
26   and bits starting at a first bit of the current packet
27   register, and
28   (f) thereafter repeat steps (b), (c), (d) and (e).

1   37. (New) The method of Claim 2, wherein the transmission
2   clock rate is greater than the data processor clock rate.

1   38. (New) The method of Claim 1, wherein the second fixed
2   size is larger in size than the first fixed size.

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1   39.   (New) The method of Claim 38, wherein the transmission

2 clock rate is less than the data processor clock rate.

1   40.   (New) The method of claim 31, wherein:

2   said step of receiving the plurality of first information

3 blocks and arranging the emulation information contained therein

4 into a plurality of second information blocks wherein

5   said step (b) of sequentially selecting a group of the

6   second fixed size bits and said step (e) of selecting a group

7   of second fixed size bits stall if there is no first

8   information block stored in either said current packet

9   register or in said last packet register.

1   41.   (New) The method of claim 31, wherein:

2   said step of receiving the plurality of first information

3 blocks and arranging the emulation information contained therein

4 into a plurality of second information blocks wherein

5   said step (a) of storing a current first information

6   block in a current packet register and said step (d) of

7   storing a next first information block in the current packet

8   register stores NOP bits if no first information block is

9   available,

10   said step (b) of sequentially selecting a group of the

11   second fixed size bits and said step (e) of selecting a group

12   of second fixed size bits selects a group of a second fixed

13   size bits with a last valid first information block stored in

14   said current packet register or in said last packet register

15   and thereafter stalls if there is no first information block

16   stored in either said current packet register or in said last

17   packet register.

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1   42. (New) The method of claim 31, wherein:

2   said step of receiving the plurality of first information

3   blocks and arranging the emulation information contained therein

4   into a plurality of second information blocks wherein

5   said step (a) of storing a current first information

6   block in a current packet register and said step (d) of

7   storing a next first information block in the current packet

8   register stores NOP bits if no first information block is

9   available,

10   said step (b) of sequentially selecting a group of the

11   second fixed size bits and said step (e) of selecting a group

12   of second fixed size bits selects a group of a second fixed

13   size bits selects all NOP bits if there is no first

14   information block stored in either said current packet

15   register or in said last packet register.

1   43. (New) The integrated circuit of Claim 17, wherein the

2   transmission clock rate is greater than the data processor clock

3   rate.

1   44. (New) The integrated circuit of Claim 16, wherein said

2   second fixed size is greater in size than said first fixed size.

1   45. (New) The integrated circuit of Claim 44, wherein the

2   transmission clock rate is less than the data processor clock rate.

1   46. (New) The integrated circuit of claim 33, wherein:

2   said combiner is further operable to

3   not sequentially select groups of the second fixed size

4   bits (b), not select a group of second fixed size bits (e) and

5   stall if there is no first information block stored in either

6   said current packet register or in said last packet register.

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1   47.   (New) The integrated circuit of claim 33, wherein:
2   said combiner is further operable to
3   store NOP bits in a current packet register (a) and store
4   NOP bits in the current packet register if no first
5   information block is available,
6   sequentially select a group of the second fixed size bits
7   (b) and select a group of second fixed size bits (e) by
8   selecting a group of a second fixed size bits with a last
9   valid first information block stored in said current packet
10   register or in said last packet register and thereafter
11   stalling if there is no first information block stored in
12   either said current packet register or in said last packet
13   register.

1   48.   (New) The integrated circuit of claim 33, wherein:
2   said combiner is further operable to
3   store NOP bits in a current packet register (a) and store
4   NOP bits in the current packet register if no first
5   information block is available,
6   sequentially select a group of the second fixed size bits
7   (b) and select a group of second fixed size bits (e) by
8   selecting all NOP bits if there is no first information block
9   stored in either said current packet register or in said last
10   packet register.

1   49.   (New) The data processing system of Claim 34, wherein:
2   the transmission clock rate is greater than the data processor
3   clock rate.

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1   50.   (New) The data processing system of Claim 27, wherein:
2   said second fixed size is greater in size than said first
3   fixed size.

1   51.   (New) The data processing system of Claim 50, wherein:
2   the transmission clock rate is less than the data processor
3   clock rate.

1   52.   (New) The data processing system of claim 36, wherein:
2   said combiner is further operable to
3   not sequentially select groups of the second fixed size
4   bits (b), not select a group of second fixed size bits (e) and
5   stall if there is no first information block stored in either
6   said current packet register or in said last packet register.

1   53.   (New) The data processing system of claim 36, wherein:
2   said combiner is further operable to
3   store NOP bits in a current packet register (a) and store
4   NOP bits in the current packet register if no first
5   information block is available,
6   sequentially select a group of the second fixed size bits
7   (b) and select a group of second fixed size bits (e) by
8   selecting a group of a second fixed size bits with a last
9   valid first information block stored in said current packet
10   register or stored in said last packet register and thereafter
11   stalling if there is no first information block stored in
12   either said current packet register or in said last packet
13   register.

1   54.   (New) The data processing system of claim 36, wherein:
2   said combiner is further operable to

3   store NOP bits in a current packet register (a) and store
4   NOP bits in the current packet register if no first
5   information block is available,
6   sequentially select a group of the second fixed size bits
7   (b) and select a group of second fixed size bits (e) by
8   selecting all NOP bits if there is no first information block
9   stored in either said current packet register or in said last
10   packet register.

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